Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**3 2 1 28 27**

**13 14 15 16 17 18**

**.151”**

**.073”**

**MASK**

**REF**

**BVA093B**

**PAD FUNCTION:**

1. **VDD**
2. **DB**
3. **NC**
4. **S8B**
5. **S7B**
6. **S6B**
7. **S5B**
8. **S4B**
9. **S3B**
10. **S2B**
11. **S1B**
12. **GND**
13. **NC**
14. **NC**
15. **A2**
16. **A1**
17. **A0**
18. **EN**
19. **S1A**
20. **S2A**
21. **S3A**
22. **S4A**
23. **S5A**
24. **S6A**
25. **S7A**
26. **S8A**
27. **VSS**
28. **DA**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0031” X .0031”**

**Backside Potential: FLOATING**

**Mask Ref: BV A093B**

**APPROVED BY: DK DIE SIZE .073” X .151” DATE: 4/20/17**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: ADG407**

**DG 10.1.2**

#### Rev B, 7/1